What is claimed is:

1. A method of fabricating a thyristor memory, comprising:

forming sidewalls in a layer of dielectric over a layer of semiconductor material to define a trench and expose a region of the semiconductor material through the opening of the trench;

forming conductive material on at least portions of the dielectric and in the trench;

patterning the conductive material to define first and second shoulders extending outwardly from the trench over regions of the dielectric outside the trench;

the patterning to comprise forming the first shoulder as an overhang extending laterally outward from the trench over regions of the layer of semiconductor material for the thyristor;

etching exposed regions of the layer of dielectric to form an implant mask while using the conductive material with the first and second shoulders as an etch mask;

implanting regions of the layer of semiconductor material; and

using the implant mask to align placement of dopant during at least a portion of the implanting.

2. The method of claim 1, in which the implanting comprises performing a first implant of first conductivity type dopant.

3. The method of claim 2, in which the first implanting comprises penetrating with the dopant of the first conductivity type regions of the layer of semiconductor material beneath an edge of the implant mask.

4. The method of claim 2, in which the first implanting comprises:

forming a base region to the thyristor; and

forming at least a portion of the base region beneath the first shoulder.

5. The method of claim 4, in which the implanting further comprises performing a second implant of second conductivity type dopant aligned with the implant mask and forming an anode/cathode-emitter.

6. The method of claim 5, in which the forming the trench comprises:

patterning first sacrificial material to cover a portion of the layer of semiconductor material to be associated with the trench;

layering dielectric over the semiconductor material and the patterned first sacrificial material;

planarizing at least one of the dielectric and the patterned first sacrificial material to form substantially equivalent heights therefor; and

after the planarizing, removing the patterned first sacrificial material to expose sidewalls of the dielectric and define the trench at least in part by the exposed sidewalls.

7. The method of claim 6, in which the forming the trench further comprises forming spacers of second dielectric against the sidewalls of the first dielectric, the spacers to narrow a width for the trench.

8. The method of claim 7, further comprising:

etching a portion of the semiconductor material exposed at a floor of the trench; and

recessing the floor of the trench relative to a plane defined by a surface of the semiconductor material outside the trench.

9. The method of claim 7, further comprising, before forming the conductive material, forming gate oxide over the exposed regions of the semiconductor material.

10. The method of claim 7, in which the etching the exposed regions of the dielectric comprises:

anisotropically etching the dielectric using the patterned conductive material as an etch mask; and

stopping the anisotropic etching after exposing a surface region of the semiconductor material.

11. The method of claim 10, further comprising:

removing material of the dielectric beneath the second shoulder; and

leaving at least a portion of the dielectric beneath the first shoulder.

12. The method of claim 11, in which the removing the material of the dielectric comprises:

isotropically etching the dielectric until exposing at least a portion of the spacer beneath the second shoulder; and

selectively etching the material of the dielectric using an etchant more favorable to etching the dielectric than either one of the semiconductor material and the second dielectric of the spacer.

13. The method of 12, in which:

the first implanting comprises using an acute angle of incidence for the first conductivity type dopant;

the second implanting comprises using a substantially orthogonal angel of incidence for the second conductivity type dopant; and

the first and second implanting define a width for the base region that is less than the lateral extent of the first shoulder.

14. The method of claim 12, further comprising:

forming source, drain and body regions for an access transistor in the layer of semiconductor material;

forming a second emitter to the thyristor of first conductivity type in the layer of semiconductor material at a side of the conductive material opposite the first emitter; and

forming the second emitter in common with one of the source and drain regions of the access transistor.

15. The method of claim 14, in which the forming the second emitter and the forming the first base region define therebetween a second base region for the thyristor in the layer of semiconductor material, the second base region disposed in the layer of semiconductor material beneath the floor of the trench and between lateral edges of the respective first base and second emitter regions.

16. The method of claim 5, further comprising:

siliciding exposed regions of the layer of semiconductor material; and

using the implant mask during the siliciding to protect masked regions of the layer of semiconductor material.

17. The method of claim 16, further comprising:

implanting carrier lifetime adjustment species to affect leakage characteristics of the first emitter region; and

using the implant mask during the implanting of the carrier lifetime adjustment species to define an extent therefore.

18. The method of claim 16, in which the siliciding further comprises siliciding-exposed surface regions of the conductive material including exposed surface regions of the patterned first and second shoulders.

19. The method of claim 5, further comprising:

forming a layer of silicon as the layer of semiconductor material over an insulator;

the first implanting comprises penetrating a full-depth of the layer of silicon with the dopant of the first conductivity type; and

the second implanting comprises penetrating at least a partial depth of the layer of silicon with the dopant of the second conductivity type.

20. A method of fabrication comprising:

patterning first sacrificial material over a layer of silicon of first conductivity type, the patterning to define an opening to expose first select regions of the layer of silicon;

forming second sacrificial material over the first sacrificial material and the layer of silicon;

planarizing the second sacrificial material and exposing an upper surface of the first sacrificial material, the planarizing to leave portions of the second sacrificial material over the first select regions of the layer of silicon;

removing the first sacrificial material and exposing sidewalls of the second sacrificial material and defining an opening therethrough to expose a second select region of the layer of silicon;

forming spacers against the sidewalls of the second sacrificial material and narrowing the opening;

forming conductive material over the layer of silicon, the second sacrificial material and the spacers;

patterning the conductive material, the patterning to comprise:

forming a body portion in the opening between the spacers,

forming first and second shoulders contiguous with the body portion; and

forming the shoulders over the spacers and over regions of the second sacrificial material outside the opening;

etching exposed regions of the second sacrificial material; and

defining the exposed regions of the second sacrificial material to be etched during the etching by using the body and the first and second shoulders of the patterned conductive material; and

forming a base region of second conductivity type for defining part of a thyristor in the layer of silicon beneath at least a portion of the second shoulder.

21. The method of claim 21, in which the etching is anisotropic and performed for a duration sufficient to expose regions of the semiconductor material.

22. The method of claim 20, in which the removing comprises selectively etching the first sacrificial material using an etchant more favorable to etching the first than the second sacrificial material.

23. The method of claim 20, in which the forming of the spacers comprises:

layering dielectric material that is resistant to metal diffusion over the second sacrificial material and conformal to the sidewalls thereof; and

anisotropically etching the layered dielectric material until exposing upper surface regions of the second sacrificial material and leaving portions thereof as the spacers against the sidewalls of the second sacrificial material.

24. The method of claim 23, in which the dielectric comprises a material having a reactivity with metal that is less favorable relative to the reactivity of the semiconductor material with the metal during formation of silicide.

25. The method of claim 20, in which the patterning the conductive material comprises:

forming a body region with a lower surface facing the layer of silicon and capacitively coupled thereto;

forming the second shoulder in contiguous relationship with the body region and overhanging the base region; and

stopping the anisotropic etching after exposing a surface region of the layer of silicon and defining a remaining portion of the second sacrificial material between the overhang of the second shoulder and the layer of silicon.

26. The method of claim 25, in which the forming the base region to the thyristor comprises:

implanting dopant of the second conductivity type into select regions of the layer of silicon using an angled implant; and

selecting an implant energy, an angle for the angled implant and a lateral extent for the second shoulder to implant dopant into the select regions of the layer of silicon with an extent extending beneath the overhang of the second shoulder to a position short of the regions beneath the body portion.

27. The method of claim 26, further comprising:

after using the second shoulder and the remaining portion of the etched second sacrificial material as an implant mask during the implanting for the base region, using the implant mask again during a substantially orthogonal implant of dopant of first conductivity type and forming an emitter region to the thyristor in the layer of silicon.

28. The method of claim 27, the formation of the base and the emitter regions further comprising:

controlling at least one of the angles for the angles of incidence and the energies of the respective base and emitter implants to form an N-P interface of the emitter relative to the base at a location beneath a peripheral edge of the implant mask.

29. The method of claim 28, further comprising:

after the implanting for the base and emitter regions, siliciding exposed regions of silicon; and

using the implant mask to protect portions of the layer of silicon during the siliciding.

30. The method of claim 29, in which the siliciding further comprises:

diffusing metal into exposed surface regions of the conductive material including the exposed surface regions of the patterned body and the first and second shoulders; and

diffusing metal into the exposed surface regions of the layer of silicon that are disposed laterally outside a peripheral edge of the remaining portion of the second sacrificial material.

31. The method of claim 30, further comprising:

implanting lifetime adjustment species into the emitter region; and

using the implant mask of the patterned conductive material and the remaining portion of the etched second sacrificial material during the implanting of the lifetime adjustment species.

32. The method of claim 29, further comprising:

forming a layer of dielectric over the layer of silicon for use as a gate/capacitor dielectric;

the forming of the conductive material to dispose the lower surface of the body portion thereof against the gate/capacitor dielectric.

33. The method of claim 25, further comprising:

after the anisotropic etching, secondly etching the second sacrificial material to remove material thereof from beneath the first shoulder; and

stopping the second etching after exposing the spacer beneath the first shoulder.

34. The method of claim 33, in which the secondly etching comprises:

isotropically etching the material of the second sacrificial material using an etchant more favorable to etching the second sacrificial material than any of the group consisting of the conductive material, the silicon and the spacer.

35. The method of claim 20, in which:

the removing of the first sacrificial material and the exposing the sidewalls of the second sacrificial material comprise defining first and second electrode openings; and

the forming and the patterning of the conductive material comprise:

forming a first portion of the conductive material to define a gate electrode in the first electrode opening;

forming a second portion of the conductive to define a capacitor electrode in the second electrode opening and with the second shoulder as a part of the capacitor electrode in contiguous relationship therewith and over regions of the second sacrificial material that neighbor the second electrode opening; and

forming the second shoulder with a lateral extent greater than that for the shoulders to the gate electrode.

36. The method of claim 35, in which:

the patterning of the first sacrificial material comprises:

defining a first portion thereof to cover a first area of the layer of silicon, the first area to be associated with the first electrode window, and

defining a second portion thereof to cover a second area of the layer of silicon, the second area to be associated the second electrode window; and

the method further comprises:

implanting at least one of extension and halo impurity species into the layer of silicon at regions defined at least in part by the patterned first portion of the first sacrificial material; and

protecting regions of the silicon proximate the second portion during the at least one of the extension and the halo implantings.

37. The method of claim 36, further comprising:

implanting dopant to define at least one of the source and drain regions in the layer of silicon while using at least the first portion patterned from the first sacrificial material as an implant mask.

38. The method of claim 37, further comprising:

during the implanting for the source and drain regions, protecting regions of the silicon layer at a side of the second portion of the patterned first sacrificial material that is opposite to the first portion.

39. A method of fabricating a memory device, comprising:

forming a plurality of wordlines over a substrate;

using a first wordline of the plurality to define, at lease in part, an access transistor in a first portion of the substrate;

using a second wordline of the plurality to define, at least in part, a capacitor electrode capacitively coupled to a first base region for a thyristor in a second portion of the substrate;

implanting first type conductivity dopant with an acute angle of incidence to form a second base region of the thyristor, the implanting to define a boundary to the second base region related to a lateral extent associated with the second wordline; and

implanting second type conductivity dopant with a substantially orthogonal angle of incidence to form an emitter region of the thyristor, the implanting to define a boundary to the emitter region related to the lateral extent associated with the second wordline.

40. The method of claim 39, in which the implanting for the first and the second type conductivity dopants form a P-N junction at the boundary between the emitter region and the second base region.

41. The method of claim 39, further comprising protecting portions of the substrate for the access transistor during the implanting for the second base region and during the implanting for the emitter region.

42. The method of claim 39, in which the forming the wordlines comprises:

patterning first sacrificial material over a top surface of the substrate to form sidewalls thereof for defining outlines between protected and exposed regions of the substrate;

implanting via the exposed regions of the substrate to form at least one of source, drain and extension regions for the access transistor;

forming second sacrificial material over the exposed regions of the substrate as defined by the sidewalls of the first sacrificial material;

planarizing at least one of the first and second sacrificial materials to establish substantially equal heights therefor;

removing the first sacrificial material and exposing sidewalls of the second sacrificial material to define first and second electrode windows therethrough, the first and second electrode windows to outline at least in part respective first and second wordline regions over the substrate;

forming spacers against the sidewalls of the second sacrificial material;

layering conductive material over the second sacrificial material and over regions of the substrate between the spacers within the first and second electrode windows;

patterning the conductive material to define first and second shoulders that extend outwardly over the spacers and over neighboring regions of the second sacrificial material proximate the electrode windows;

etching exposed regions of the second sacrificial material;

using the patterned conductive material with the first and second shoulders as an etch mask to define the exposed regions of the second sacrificial material;

stopping the etching after removing at least a substantial thickness of the exposed regions of the sacrificial material and forming a remaining portion of the second sacrificial material between the substrate and at least one of the first and second shoulders of the second wordline; and

using the remaining portion of the second sacrificial material together with the associated one of the first and second shoulders thereover as a protective mask during the implanting for the second base.

43. The method of claim 43, further comprising:

protecting the second portion of the substrate for the thyristor;

defining exposed regions of the substrate at least in part by the first portion of the patterned first sacrificial material; and

forming an extension for the access transistor by implanting first type conductivity dopant into the exposed regions of the substrate defined at least in part by the first portion of the patterned first sacrificial material.

44. The method of claim 43, in which the implanting with the first conductivity type dopant forms one of the source and drain regions to the access transistor in common with a cathode/anode-emitter for the thyristor.

45. The method of claim 44, further comprising:

using silicon on insulator (SOI) structure for the substrate;

the implantings to form the drain, source, emitter and base regions for the respective portions of the access transistor and the thyristor within the layer of silicon of the SOI structure.

46. The method of claim 45, in which the spacers comprise nitride and the second sacrificial material comprises oxide.

47. The method of claim 42, in which the removing the first sacrificial material to define the first and second electrode windows comprises:

selectively etching the first sacrificial material more favorably relative to the second sacrificial material;

exposing sidewalls of the second sacrificial material; and

using the exposed sidewalls of the second sacrificial material to define, at least in part, the first and second electrode windows.

48. The method of 47, further comprising:

etching a recess into the substrate; and

forming the recess with an outline defined at least in part by at least one of the first and second electrode windows.

49. The method of claim 42, further comprising siliciding conductive material of the wordlines after the implantings for the base and emitter regions.

50. The method of claim 49, further comprising using an anneal to activate the implants of the base and emitter regions before the siliciding.

51. A method of fabricating a thin capacitively coupled thyristor memory device, the method comprising:

forming a first wordline over a substrate for a gate electrode to an access transistor;

forming a second wordline over the substrate for a capacitor electrode to be capacitively coupled to a first base region of a thyristor;

implanting first type conductivity dopant in the substrate using an acute angle of incidence to form a second base region of the thyristor aligned at least in part relative to a shoulder of the second wordline; and

implanting second type conductivity dopant in the substrate using a substantially orthogonal angle of incidence to form an emitter region of the thyristor aligned relative to the shoulder of the second wordline.

52. The method of claim 51, further comprising protecting regions of the substrate to be associated with the access transistor during the respective implantings for the second base and emitter regions.

53. The method of claim 51, in which the formation of the wordlines comprises using replacement gate processes.

54. The method of claim 51, in which the forming the wordlines comprises:

forming first sacrificial dielectric over the substrate to define a pre-gate electrode, a pre-capacitor electrode and exposed surface areas of the substrate about and between the pre-gate and pre-capacitor electrodes;

implanting source/drain implants for the access transistor while using the pre-gate electrode as a mask and while protecting regions of the substrate to be associated with at least part of the thyristor;

forming second sacrificial dielectric over the exposed surface areas of the substrate about and between the pre-gate and the pre-capacitor electrodes;

removing the first sacrificial dielectric and exposing sidewalls of the second sacrificial dielectric to define first and second windows therethrough;

forming spacers against the sidewalls of the second sacrificial dielectric and narrowing the first and second openings;

forming conductive material in the openings between the spacers and also over flange regions of the second sacrificial dielectric that meet the edges of the windows;

patterning the conductive material to define the wordline for the capacitor electrode with first and second shoulders over the flange regions of the second sacrificial dielectric that neighbored the windows; and

forming at least one of the first and second shoulders of the capacitor electrode over a portion of the second sacrificial dielectric that extends over the base region; and

etching regions of the second sacrificial dielectric that are exposed and located beyond at least one of the first and second shoulders, the etching to define a remaining portion of the second sacrificial dielectric as an implant mask with a lateral extent over the region for the base of the thyristor.

55. The method of claim 54, further comprising:

forming gate oxide over surface regions of the substrate for insulating the conductive material for the wordlines to be formed thereover;

after the implantings, siliciding exposed regions of the substrate associated with the emitter and source/drain regions; and

using the remaining portion of the second sacrificial dielectric to protect surface areas over at least portions of the base regions for the thyristor during the siliciding.

56. The method of claim 55, further comprising implanting carrier lifetime adjustment species into the emitter region of the thyristor aligned at least in part relative to the implant mask formed by the remaining portion of the second sacrificial dielectric.

57. A method of fabricating a semiconductor device, comprising;

forming first and second wordline electrodes over a layer of silicon;

forming at least one of the first and second wordline electrodes with a gull-wing structure; and

forming first and second base regions and anode and cathode-emitter regions for a thyristor in the layer of silicon;

forming each of the interface between the first and second base regions and the interface between the second base region and the anode/cathode-emitter region for the thyristor with an alignment related at least in part to a lateral extent for the gull wing.

58. The method of claim 57, further comprising:

forming a source/drain region for an access transistor in the layer of silicon laterally between the first and second electrodes; and

forming the source/drain region in common with a cathode/anode-emitter to the thyristor.

59. The method of claim 58, in which the forming the first and second wordlines comprises using a replacement gate process, which comprises defining slotted footprint locations between sidewalls of dielectric for at least portions of the wordlines to be formed over the layer of silicon.

60. The method of claim 59, in which defining the slotted footprint locations for the wordlines by the replacement gate process comprises:

forming a first replacement gate over a region of the layer of silicon for the first wordline;

forming a second replacement gate over regions of the layer of silicon for the second wordline;

layering dielectric over select regions of the layer of silicon, the select regions defined outside and between the first and second replacement gates;

removing the replacement gates to expose sidewalls of the layered dielectric and defining first and second slots; and

layering conductive material in the first and second slots that are defined at least in part by the sidewalls of the layered dielectric;

the layering the conductive material to further form portions thereof over regions of the dielectric neighboring the slots.

61. The method of claim 60, further comprising, before removing the replacement gates, planarizing the layered dielectric and exposing upper surface regions of the replacement gates.

62. The method of claim 60, further comprising, before the layering of the conductive material in the first and second slots:

etching exposed regions of the layer of silicon to form a recess therein;

forming the recess with an outline defined by sidewalls for the first and second slots; and

lining the recesses with dielectric to insulate the layer of silicon from the electrodes to be formed thereover.

63. The method of claim 60, further comprising:

patterning the layered conductive material to define a gate electrode in the first slot for the first wordline electrode and a capacitor electrode in the second slot for the second wordline electrode;

the patterning to define the capacitor electrode with gull wings that extend outward from the second slot and over upper surface regions of the dielectric proximate and meeting the sidewalls associated with defining the second slot.

64. The method of claim 63, further comprising:

before layering the conductive material in the first and second slots, forming spacers against the sidewalls to narrow the respective slots.

65. The method of claim 63, in which the forming the first and second base regions comprise:

implanting dopant for the second base region in the layer of silicon using an acute angle of incidence; and

aligning the implanting for the second base region at least in part relative to a peripheral edge of the dielectric that is distant the previously defined second slot and distant the previously defined first slot;

the implanting for the second base region comprises:

penetrating regions of the layer of silicon beneath the dielectric but laterally clear of the second slot; and

forming an N-P interface between the second base region relative to a first base region, which extends contiguously from the first base region in the layer of silicon and laterally toward and beneath the second slot.

66. The method of claim 65, in which the forming the anode/cathode-emitter for the thyristor comprises:

implanting dopant for the anode/cathode-emitter region in the layer of silicon using a substantially orthogonal angle of incidence; and

aligning the implanting for the anode/cathode-emitter region at least in part relative to the peripheral edge of the dielectric that is distant the first and the second slots;

the implanting for the anode/cathode-emitter comprises:

forming an N-P interface between the anode/cathode-emitter and the second base region; and

defining a width of the second base region for the thyristor beneath the dielectric.

67. The method of claim 66, in which the forming the cathode/anode-emitter for the thyristor comprises:

using a substantially orthogonal angle of incidence during the implanting of dopant for the source/drain region for the access transistor;

the implanting for the source/drain region to be performed in common with that for the cathode/anode-emitter region; and

aligning the implanting for the cathode/anode-emitter region and the source/drain region relative to the edges of the respective first and second replacement gates.

68. The method of claim 67, in which the forming the cathode/anode-emitter region for the thyristor in common with the source/drain region further comprises:

protecting other regions of the layer of silicon associated with the thyristor during the implanting.

69. The method of claim 58, in which the forming the second base region comprises, before removing the replacement gates:

implanting dopant for the second base region in the layer of silicon beneath a peripheral edge of the dielectric using an angled implant; and

implanting dopant for the anode/cathode-emitter region in the layer of silicon aligned to the peripheral edge of the dielectric and using a substantially orthogonal implant; and

defining a width for the second base region by controlling a difference between the angles associated with the substantially orthogonal implant and the angled implant.

70. The method of claim 69, further comprising, before removing the replacement gates:

planarizing at least one of the layered dielectric and the replacement gates and exposing upper surface regions of the replacement gates;

patterning photoresist over the planarized dielectric and the first and second replacement gates;

using the patterned photoresist to protect regions over the layer of silicon to be associated with the access transistor, and first and second base regions for the thyristor;

using the patterned photoresist to define exposed regions of the layered dielectric over portions of the layer of silicon to be associated with the anode/cathode-emitter for the thyristor; and

etching the exposed regions of the layered dielectric as defined by the patterned photoresist and forming the peripheral edge thereof;

the peripheral edge to be used to assist the alignment of the implants for the second base region and the anode/cathode-emitter region.

71. The method of 57, further comprising activating implants of the source, drain, base and emitter regions for the access transistor and for the thyristor before the full formation of the first and second wordlines.

72. The method of 71, further comprising:

forming at least part of the respective first and second wordlines with polysilicon; and

siliciding surface regions of the polysilicon for the first and second wordlines;

starting the siliciding after the activating of the dopants.

73. The method of claim 72, further comprising:

siliciding exposed regions of the layer of silicon; and

using dielectric over a lateral extent of the layer of silicon beneath the gull wing associated with the interface alignment, to define at least in part the protected and exposed regions of the layer of silicon during the siliciding.

74. A memory device comprising:

a layer of silicon over an insulator;

cathode/anode-emitter, first base, second base and anode/cathode emitter regions of a thyristor disposed contiguously and in electrical series relationship in the layer of silicon;

source/drain, channel and drain/source regions for a transistor disposed contiguously and in electrical series relationship in the layer of silicon;

one of the anode and cathode-emitter regions in common with one of the source and drain regions;

a gate electrode disposed in insulated relationship over the channel region for the transistor; and

a capacitor electrode disposed in insulated relationship over the first base region of the thyristor;

the capacitor electrode comprising a "T" structure replacement gate having:

a foot disposed over and capacitively coupled to the first base region of the thyristor,

a leg extending upward from the foot, and

at least one wing disposed across and extending outwardly from the top of the leg;

one of the wings of the capacitor electrode to overhang at least a portion of the first and second base regions for the thyristor.

75. The memory device of claim 74, in which:

the gate electrode for the transistor comprises conductive material that is shaped, per a cross-section thereof, to define a T-structure;

the T-structure for the gate electrode comprising:

a leg, and

wings connected to and extending outwardly from the top of the leg;

the leg of the T-structured gate electrode slotted between walls of dielectric to position a foot of the leg above the channel region for the transistor; and

each of the capacitor and gate electrodes further comprising silicide on their upper and outwardly facing surfaces.

76. The memory device of claim 75, further comprising:

silicide resistant dielectric beneath at least one of first and second wings associated with the overhang of the capacitor electrode; and

silicide on a surface of the layer of silicon the anode/cathode-emitter region of the thyristor;

the silicide at the anode/cathode-emitter region comprising a peripheral edge meeting a sidewall of the silicide resistant dielectric.

77. The memory device of claim 76, in which:

the overhanging of the wing of the capacitor electrode comprises an edge disposed laterally distant the leg;

the sidewall of the silicide resistant dielectric related to the laterally distant edge of the overhanging wing; and

the second base region of the thyristor comprising an extent in the layer of silicon defined at least in part in relationship to the sidewall of the silicide resistant dielectric.

78. The memory device of claim 77, in which:

the second and first base regions define a first N-P junction therebetween;

the first N-P junction meeting a surface of the layer of silicon to define an outline beneath the silicide resistant dielectric, the outline laterally offset from the sidewall of the silicide resistant dielectric; and

the anode/cathode-emitter and the second base region define a separate N-P junction therebetween;

the second N-P junction meeting a surface of the layer of silicon to define an outline therefore located laterally beneath the silicide resistant dielectric and laterally short of the outline for the first N-P junction.

79. A system comprising:

a processor;

memory; and

a bus to transfer data between the processor and the memory;

at least a portion of the memory comprising thin capacitively coupled thyristor (TCCT) memory, the TCCT memory comprising:

a layer of silicon over an insulator;

cathode/anode-emitter, first base, second base and anode/cathode emitter regions of a thyristor disposed contiguously and in electrical series relationship in the layer of silicon;

source/drain, channel and drain/source regions for a transistor disposed contiguously and in electrical series relationship in the layer of silicon;

one of the anode and cathode-emitter regions in common with one of the source and drain regions;

a gate electrode disposed in insulated relationship over the channel region for the transistor; and

a capacitor electrode disposed in insulated relationship over the first base region of the thyristor;

the capacitor electrode comprising conductive material shaped as a T-structure, the T-structured conductive material comprising:

a foot portion to the T-structure presenting a lower surface disposed over and capacitively coupled to the first base region of the thyristor,

a leg portion extending upward from the foot portion, and

first and second wing portions extending laterally outward from a top of the leg portion;

one of the first and second wing portions of the T-structured capacitor electrode disposed as an overhang over at least a portion of the first and second base regions.

80. The system of claim 79, in which the first and second wordline electrodes each comprise the conductive material formed with the T-structure;

the leg to the T-structured conductive material of the first wordline slotted in a trench over a channel region for the access transistor; and

the leg to the T-structured conductive material of the second wordline slotted in a trench over a base region for the TCCT.

81. The system of claim 80, in which the leg of the T-structured capacitor electrode comprises a lower surface disposed over and capacitively coupled to a first base region for the thyristor, the T-structured capacitor electrode further comprises first and second shoulders extending outwardly from the top of the leg; one of the shoulders having a lateral extent that overhangs a portion of the first base region and the second base region for the thyristor.

82. The system of claim 81, further comprising silicide resistant dielectric between the overhanging shoulder of the capacitor electrode and the corresponding portion of the first base and the second base regions.

83. The system of claim 82, further comprising:

silicide on an anode/cathode-emitter region of the thyristor in the layer of silicon;

the silicide resistant dielectric comprising a sidewall meeting a peripheral edge of the silicide on the anode/cathode-emitter;

the second base region comprising a width at the surface of the layer of silicon beneath the silicide resistant dielectric and laterally clear of the silicide.

84. The system of 83, further comprising:

a reference line to receive a reference voltage;

a reference contact to electrically couple between the reference line and the silicide on the anode/cathode-emitter;

a bitline to propagate a bit signal; and

a bitline contact to electrically couple between the bitline and the drain/source region of the access transistor.

85. A semiconductor device comprising:

a thyristor having first and second base regions disposed serially between first and second emitter regions;

a capacitor electrode comprising a surface disposed over at least one of the first and second base regions;

dielectric of first thickness disposed between the surface of the capacitor electrode and the first base region;

dielectric of second thickness disposed between the second base region and the surface of the capacitor electrode;

the dielectric of second thickness substantially thicker than that of the first thickness.

86. The device of claim 85, the dielectric of second thickness comprising a thickness that is at least twice that of the dielectric of the first thickness.

87. The device of claim 86, a portion of the dielectric of the second thickness also between a portion of the first base region and the surface of the capacitor electrode.

88. The device of claim 86, the dielectric of first thickness comprising a thickness less than 20nm, and the dielectric of second thickness comprising a thickness greater than 50nm.

89. The device of claim 85, further comprising:

a transistor comprising source and drain regions separated by a channel region, and a gate electrode to control a conductivity of the channel region; and

one of the source and drain regions of the MOSFET in common with one of the first and second emitter regions of the thyristor.

90. The device of claim 89, the capacitor electrode that is coupled to the thyristor and the gate electrode of the transistor each formed by a replacement gate process.

91. The method of claim 89, the gate electrode comprising a replacement gate having a T-structure having a lower end facing the channel region of the transistor, the arms of the T-structure extending laterally outward from an upper end of the leg.

92. The device of claim 91, the capacitor electrode per a cross-section thereof comprising:

a foot disposed in spaced relationship over at least a portion of the first base region of the thyristor and separated therefrom by the dielectric of first thickness,

a body extending upwardly from the foot, and

at least one arm extending laterally outward from the body,

one of the arm(s) over a portion of the second base and spaced therefrom, at least in part, by the dielectric of the second thickness.

93. The device of claim 92, the emitter and base regions of the thyristor formed in a layer of silicon of an SOI substrate.

94. The method of claim 93, the second base region of the thyristor meeting a surface of the silicon layer to define a width between the first base region and its neighboring emitter region,

the full width of the second base region, as presented at the surface of the silicon layer, beneath the dielectric of the second thickness.

95. The device of claim 94, in which a portion of the emitter region of the thyristor that neighbors, the second base region is disposed beneath the dielectric of the second thickness.

96. The device of claim 95, in which the base-emitter junction defined between the emitter region and the second base region, is self-aligned to a lateral edge of the dielectric of the second thickness.

97. The device of claim 96, further comprising silicide over the emitter region, the silicide comprising an outline defined in part by the lateral edge of the dielectric of second thickness.

98. The device of claim 85, in which the dielectric of first thickness comprises:

a barrier layer; and

a high-K dielectric conformal to the barrier layer.

99. The device of claim 98, in which the barrier layer comprises a thermal oxide of thickness less than 5nm.

100. The device of claim 99, in which the high-k dielectric comprises a dielectric constant greater than that of the oxide.

101. The device of claim 100, in which the high-k dielectric defines a conformal layer of thickness less than 5 nm over the barrier layer.